Notice of Allowability	Application No.	Applicant(s)	
	09/841,799	HO ET AL.	
	Examiner	Art Unit	
	Sam Rizk	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *5/7/2007*.

2. ☒ The allowed claim(s) is/are *1,2,5-42*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

GUY LAMARRE
PRIMARY EXAMINER

DETAILED ACTION

- Response to the applicant's amendment dated 5/7/2007
- Claims 3-4 have been cancelled
- Amended claims 1,2 and 5-42 have been submitted for examination
- Claims 1,2 and 5-42 have been allowed

Response to Arguments

1. Applicant's arguments and amendment of claim 1, see page 9, filed on 5.7.2007, with respect to claim 1have been fully considered and are persuasive. The rejection of claim 1 has been withdrawn.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

2. The prior Art of record and in particular Kuwata US patent no. 6595707 (Hereinafter Kuwata) do not teach, suggest, or otherwise render obvious the limitations recited in claim 1 that:

a parity module configured to receive certain input bits from one of the binary number sequence and a previous column and to calculate the parity of the certain input bits; and

a delay module configured to receive other input bits from one of the binary number sequence and a previous column and to delay the other input bits~

wherein **the parity modules form the last column of the modules,**

the first column of modules to the second to last column of modules forms

an inner array having an equivalent number of rows and columns of modules, and within the inner array of modules the parity modules form a diagonal of the inner array from a first row to a last row and the delay modules are the remaining modules within the inner array.

3. Claims 2 and 5-26 depend from claims 1.

4. Claims 27—42 have been allowed in the office action filed on 6/13/2006 and copied below in its entirety.

Claim 27 cite similar language to claim 1(correction: should read claim 4):
A circuit to calculate the cumulative parity of a binary limber sequence, comprising:
- an array of delay elements, the delay elements aligned to form M + 1 columns and M rows within the array, where M represents a number of parallel input bit values, and wherein the array is configured to receive the binary number sequence at the first column of the delay elements and to produce the cumulative parity as output at the (M+l)th column of the delay elements, the array comprising:
- diagonal delay elements forming a diagonal of an M column by M row inner array of the array, from the first row and the first column to the Mth row and the Mth column of the array; non-diagonal delay elements, wherein the non-diagonal delay
elements are the remaining delay elements within the inner array; and the (M+l)th column delay elements;
- diagonal gate elements located from the second row through the Mth rows of the array to calculate parity information, the diagonal gate elements each having a diagonal gate output connected to a diagonal delay input of the corresponding diagonal delay element in the same row and the next column of the array, a first diagonal gate input connected to a diagonal delay output of the corresponding diagonal delay element in the prior row and the previous column of the array, and a second diagonal gate input connected to a non-diagonal delay output of the corresponding non-diagonal delay element in the same row and the previous column of the array; and
-column gate elements located from the first row to the Mth row of the

array and between the Mth column and the (M+I)th column of the array, the column gate elements each having a column gate output connected to a column delay input of the corresponding (M+I)th column delay element in the same row of the array, the column gate elements used to pass the parity information from the diagonal and non-diagonal outputs of respective diagonal and non-diagonal delay elements in prior columns of the array to the (M+I)th column delay elements.

5. Claims 28-32 depend from claim 27.

6. Claim 33 cite similar language to claim 1 (Correction: should read claim 4):
A method of using an array of M(M+I) modules to calculate the cumulative parity of a binary number sequence, the array comprising M rows of M+I modules and M+I columns of M modules, the method comprising: within a first clock cycle T: calculating the cumulative parity of a first input group of n input bit values and a first initial parity input value at the first row first column module; delaying a second input group of n input bit values at the second row first column module; and delaying an Mth input group of n input bit values at the Mth row first column module; within a second clock cycle 2T: delaying the cumulative parity of the first input group at the first row second column module; calculating the cumulative parity of the second input group and a second initial parity input bit value at the second row second column module; and delaying the Mth input group at the Mth row second column module; within an Mth clock cycle MT:
delaying the cumulative parity of the first input group at the first row Mth column module; delaying the cumulative parity of the second input group at the second row Mth column module; and calculating the cumulative parity of the Mth input group and an Mth initial parity input bit value at the Mth row Mth column module; and within an (M+I)th clock cycle (M+I)T: calculating a first output group of n output bit values at the first row (M+I)th column module; calculating a second output group of n output bit values at the second row (M+I)th column module; and calculating an Mth output group of n output bit values at the Mth row (M+I)th column module.

7. Claims 34-40 depend from claim 33.

8. Claims 41 and 44 cite similar language to claim 33.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk, MSEE, ABD

Examiner

ART UNIT 2112

5/16/07

GUY LAMARRE
PRIMARY EXAMINER